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| 10/673,583 | 09/30/2003 | Andrej S. Mitrovic | 230420US6YA | 1606 |

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| EXAMINER | |
|---|---|
| SAXENA, AKASH | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/673,583 | MITROVIC, ANDREJ S. | |
| | Examiner | Art Unit | |
| | Akash Saxena | 2128 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claim(s) 1-65 has/have been presented for examination based on amendment filed on 6th July 2007.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6th July 2007 has been entered.
3. Claim(s) 62 is/are amended.
4. Claim(s) 1-65 remain rejected under 35 USC § 112.
5. Claim(s) 1-65 remain rejected under 35 USC § 103.
6. The arguments submitted by the applicant have been fully considered. Claims 1-65 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

***Claim Rejections - 35 USC § 101 and response the applicant's remarks***

7. Examiner withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 62 in view of the applicant's amendment.

***Response to Double Patenting***

8. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,507 and 10/673,501, 10/673,138, *10/673,467 (Added)* are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

***Response to Applicant's Remarks for 35 U.S.C. § 103***

**9. Claims 1-11, 13-14, 17-19, 21-27, 28-32, 33-38, 40-41, 44-46, 48-54, 55-57 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).**

Regarding Claims 1-11, 13-14, 17-19, 21-27, 28-32, 33-38, 40-41, 44-46, 48-54, 55-57 and 60-65

**(Argument 1)** Applicant has argued the following:

> Applicant respectfully disagrees with the examiner's asserted position that it is physically not possible to have the first principle simulations of the actual process be performed at the same time with the actual process and then use the result to perform the actual process on the same wafer. Any process in a semiconductor-processing tool takes a specific amount of time to run. During this run time, the present invention can take data from the actual ongoing process and use a first principles simulation to provide a first principles simulation result in accordance with the process data, as specifically claimed. **[1]** The result could be for example a trajectory of how the process will evolve with time. The result may further as claimed be used to generate or supplement an empirical model for the reactor.
> Applicant discloses in numbered paragraph [0067] of the filed specification that **[2]**:
>
> Specification [0067]
> *[0067] However, for these statistical methods to be able to reliably sense and control the tool under widely varying operating conditions, the database must be broad-enough to cover all operating conditions, which makes the database a burden to produce. The on-tool first principles simulation capability of the present invention does not require the creation of any such database because tool response to process conditions is predicted from physical first principles directly and accurately, given accurate working models and accurate input data. However, statistical methods can still be used to refine working models and input data as more run-time information under different operating conditions becomes available, but having such information is not required by the present invention for process sensing and control capability. Indeed, the process model Can provide a basis upon which the process can be empirically controlled by using the process model to extend those known empirical solutions to "solutions" where empirical results have not been physically made. Hence, the present invention in one embodiment empirically characterizes the process tool by supplementing the known (i.e. physically observed) Solutions with first principle simulation module solutions, the simulation module solutions being consistent with the known solutions. Eventually, as better statistics develop, the simulation module solutions can be superseded by the database of empirical solutions.*
>
> Moreover, because of the Applicant's use of features as defined for example in Claims 15-21 and Claim 59, the time to perform the first principle's simulation is now commensurate with the time of

> a semiconductor process run and permits the present invention to overcome what the examiner see as an impossibility. That is, "it is physically not possible to have the first principle simulation of the actual process to be performed at same time with actual process and then use the result to perform the actual process on the same wafer." This assessment by the examiner based on the examiner's understanding of Sonderman et al, under KSR International Co. v. Teleflex Inc. et al. 2007 U.S. LEXIS 4745 (to be discussed later), should be prima facie evidence of the non-obviousness of the claims.

**(Response 1)** Examiner thanks applicant for providing clarification **[1]**, however the cited section of the specification teaches of first principle simulation model with and without database **[2]** and does not teach the argument made in **[1]** that Any process in a semiconductor-processing tool takes a specific amount of time to run. During this run time, the present invention can take data from the actual ongoing process and use a first principles simulation to provide a first principles simulation result in accordance with the process data, as specifically claimed.

Arguendo if examiner's position is incorrect, applicant asserted advantages **[1]** are not sufficient to overcome the rejection(s) of record because it is not supported by the specification.

Secondly, in view of arguments made with KSR, Lack of critical/essential elements constituting an enabling disclosure cannot be obviated with common knowledge, where the implied speed of simulation is not supported by critical details (*essential matter*) of the First Simulation Model that makes the First Simulation Model faster. In this case the claim omits the details and cannot be obvious. MPEP 2172.01 states:

> A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling. In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). See also MPEP § 2164.08(c). Such essential matter may include missing elements, steps or necessary structural cooperative relationships of elements described by the applicant(s) as necessary to practice the invention.

**(Argument 2)** Applicant has cited Sonderman Col.9 Lines 46-51

> The system 100 then optimizes the simulation (described above) ***to find more optimal process target*** (T.sub.i) **for each silicon wafer, S.sub.i.** ***to be processed***. These target values are then used ***to generate new control inputs***, X.sub.Ti, on the line 805 to control ***a subsequent process*** **of a silicon wafer S.sub.i [Emphasis added by examiner]**. The ***new control inputs***, X.sub.Ti, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like.

with the following argument:

> Thus, this section of Sonderman et al clearly discloses that the simulation is to find a more optimum process target for each silicon wafer to be processed. The simulation results produce a new control input for the silicon wafer to be processed. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process to be performed before performance of the actual process, and not the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process.***

**(Response 2)** Applicant emphasized section of Sonderman is bolded and italicized.

Examiner cited portion is bolded and underlined.

Examiner disagrees with the applicant that argument because the results of the simulation are applied to the same semiconductor. Sonderman clearly states each silicon wafer S.sub.i is exposed to new control inputs for subsequent processing (not subsequent wafer in the next round as indicated by second underlined phrase). If the intent of Sonderman not was to indicate that new control inputs generated by simulation for the actual process being performed during performance of the actual process, he would have stated it is applied to the subsequent **silicon wafer S.sub.*i+1*.**

Instead the inputs are applied to the same silicon wafer **S.sub.i**. Applicant's arguments are unpersuasive.

**(Argument 3)** Applicant has cited Fig.4 from Sonderman requiting the steps in Fig.4 and presenting the following argument.

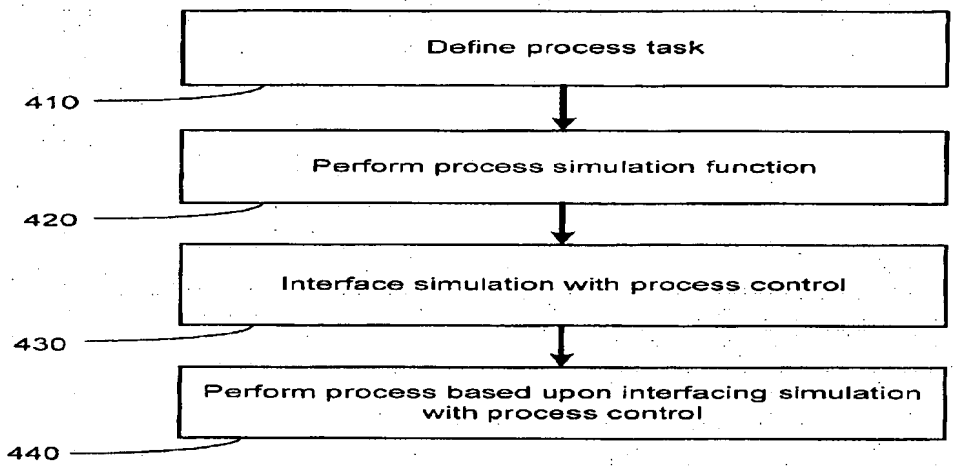


FIGURE 4

Hence, the process flow in Sonderman et al is straightforward:
1) define process to be modeled,
2) model process for simulation result,
3) interface simulation result to processor, and then
4) run the process under control based on the pre-existing simulation result.

Note also that this sequence in Sonderman et al means that Sonderman et al do not disclose inputting process data relating to an actual process being performed by the semiconductor processing tool, as also claimed. Rather, Sonderman et al use data from previous runs to produce a simulation result.

Accordingly, Applicant respectfully submits that Sonderman et al do not disclose and indeed teach away from the present invention.

**(Response 3)** Examiner thanks applicant for their interpretation, however the interpretation is incomplete with the reference that this process involves a feedback, therefore the applicant's assertion that control is based on the pre-existing simulation result and Sonderman et al does not disclose inputting process data relating to an actual process being performed by the semiconductor processing tool is incorrect. Sonderman Col.4 Line 65-Col.5 Line 10 states:

Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A feedback loop in then completed when the process control environment 180

> sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Sonderman clearly teaches inputting process data relating to an actual process being performed by the semiconductor processing tool, into the simulator and applying the simulation result to the semiconductor-processing tool.

Further in support of examiner's argument, applicant is also performing the same process of feedback modification (See specification Fig.7). In conclusion, Sonderman does not teach away from the claimed invention and applicant's arguments are found to be unpersuasive.

**(Argument 4)** Applicant has argued that Jain does not overcome the deficiencies of Sonderman.

**(Response 4)** Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant has merely cited portion of Jain without clearly showing why Jain does not overcome the deficiencies of Sonderman.

**(Argument 5)** Applicant has stated the following:

> Moreover, the proposed development work in Jain is understood better in the light of the "conventional approach" referred to by Kee et al, made of record by the Information Disclosure Statement filed December 20, 2005.

Further arguments are presented with current case law KSR International Vs. Teleflex Inc.

**(Response 5)** First, Kee et al is not used as prior art for rejecting the current invention. Secondly, examiner fails to see the connection between Jain and Kee et

al as neither of them reference to each other in any way. Thirdly, Applicant also has not further established why the so-called "conventional approach" would link them. In light of the above applicant's arguments are found to be unpersuasive. Fourthly, the limitations of being First Principle Simulation being faster than actual process is not claimed; and even if claimed does not present a limitation as what makes First Principle Simulation faster is not disclosed.

**(Argument 6)** Applicant has argued:

> In the present situation, the claimed method of performing a first principles simulation for the actual process being performed during performance of the actual process produces more than an expected result in that Sonderman et al (***in having to develop a new control inputs for each subsequent wafer***) can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process. Indeed, as pointed out above, the examiner considered it an impossibility to simultaneously perform a first principles simulation result and to control the actual process being run with the first principles simulation result **[3]**. Hence, the claimed processes and systems produce an unexpected result **[4]**.

**(Response 6)** Examiner thanks applicant for the remarks above, however the new control inputs are not developed for the processing of each subsequent wafer, but instead are for subsequent processing [performed on] a silicon wafer S.sub.i (Sonderman: Col.9 Lines 44-46 – this point is also addressed above in response to argument 1).

Further ***most importantly*** applicant is arguing limitation, which are not present in the claim and may constitute patentable subject matter. Specifically, as indicated by applicant "the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process." However, this is the conclusory statement, where what makes the

current first principle simulation model realize the real time process control possible is not claimed. Further distinguishing it from Sonderman may also help in defining a more patentable subject matter. Also see MPEP 2172.01 cited above.

Applicant has quoted examiner **[3]** bolstering their position of unexpected result **[4],** however it is only unexpected because it is not enabled in the specification – specifically what makes the First Principle Simulation faster than models disclosed in prior art is not present in the specification.

Further, applicants in arguing that "Indeed, as pointed out above, the examiner considered it an impossibility to simultaneously perform a first principles simulation result and to control the actual process being run with the first principles simulation result", render the above premise of unexpected result **[4]** false by their own admission. Applicant's argument would have merit if Applicants agreed that it was impossible. In any case, Applicants speculate but provide no evidence in the specification (See Drawings Fig.8).

Viewed differently, applicant's position on this matter is consistent with a number of the Graham factors identified in MPEP 2141 III as objective evidence of non-obviousness.

---------- End of Response to 35 USC 103 Arguments ----------

***Claim Rejections - 35 USC § 112¶1st and response the applicant's remarks***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 1-65 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued citing specification paragraphs [0035] and [0036] as to what constitutes first principle physical model.

(Response to applicant's remarks)

Applicant has provided an exact support in disclosure for such attributes in the model. Applicant has incorrectly quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling although they rely on the commercially available packages to model the various first principle simulation models, the details of the model are absent from the specification. The details of these model which lead to unexpected results (Argument & response 5) are very relevant to the designing the first principle physical model. Examiner respectfully maintains the rejection.

Further please see MPEP 2172.01 cited above.

***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,501.**

| Application No. 10/673,583 | Application No. 10/673,501 |
|---|---|
| A method of facilitating a process performed by a semiconductor processing tool, comprising: | A method of facilitating a process performed by a semiconductor processing tool, comprising: |
| inputting data relating to a process performed by the semiconductor processing tool; | inputting data relating to a process performed by the semiconductor processing tool; |
| inputting a first principles physical model relating to the semiconductor processing tool; | inputting a first principles physical model relating to the semiconductor processing tool; |
| performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and | performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a simulation result for the process performed by the semiconductor processing tool; and |
| using the virtual sensor measurement *obtained during performance of actual process* to facilitate the process performed by the semiconductor processing tool. | using the simulation result *obtained during performance of actual process* as part of a data set that characterizes the process performed by the semiconductor processing tool. |

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same

simulation result (Specification: Page 13[0051] Last sentence). Further, the process of facilitating could be a characterization the semiconductor fabrication process (Specification: Page 6[0032] Lines 1-5). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

2. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,507.**

| Application No. 10/673,583 | Application No. 10/673,507 |
|---|---|
| A method of facilitating a process performed by a semiconductor processing tool, comprising: | A method of controlling a process performed by a semiconductor processing tool, comprising: |
| inputting data relating to a process performed by the semiconductor processing tool; | inputting data relating to a process performed by the semiconductor processing tool; |
| inputting a first principles physical model relating to the semiconductor processing tool; | inputting a first principles physical model relating to the semiconductor processing tool; |
| performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and | performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a first principles simulation result; and |
| using the virtual sensor measurement *obtained during performance of actual process* to facilitate the process performed by the semiconductor processing tool. | using the first principles simulation result *obtained during performance of actual process* to control the process performed by the semiconductor processing tool.. |

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). Further, the process of facilitating is also same as providing the simulation results to control the actual

semiconductor processing tool. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,138.**

| Application No. 10/673,583 | Application No. 10/673,138 |
|---|---|
| A method of facilitating a process performed by a semiconductor-processing tool, comprising: | A method of facilitating a process performed by a semiconductor-processing tool, comprising: |
| inputting data relating to a process performed by the semiconductor processing tool; | inputting data relating to a process performed by the semiconductor processing tool; |
| inputting a first principles physical model relating to the semiconductor processing tool; | inputting a first principles physical model relating to the semiconductor processing tool; |
| performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and | performing first principles simulation *for the actual process being performed during performance of actual process* using the input data and the physical model to provide a first principles simulation result; and |
| using the virtual sensor measurement *obtained during performance of actual process* to facilitate the process performed by the semiconductor processing tool. | using the first principles simulation result *obtained during performance of actual process* to facilitate the process performed by the semiconductor processing tool. |

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Further, all the three non-statutory obviousness-type double patenting rejections for the application have substantially same or identical specification. Also, independent claims belonging different statutory category, having substantially

similar limitations, in the three co-pending applications may also have similar double patenting rejections.

11. **Further, Claim 1 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,467.**

The steps of controlling, inputting data, inputting a first principle physical model, performing simulation and selecting/using results are almost identical in the both the claim 1 sets for the co-pending applications. Other independent claims in the copending applications are rejectable similarly.

---------- End of Double Patenting Rejection ----------

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**12. Claims 1-11, 13-14, 17-19, 21-27, 28-32, 33-38, 40-41, 44-46, 48-54, 55-57 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).**

Jain Reference has been provided with the previous office action.

Regarding Claim 1 (Updated)

Sonderman teaches a method to facilitate a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting process data relating to the actual process performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; Col.7

Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool describing at least one of a basic physical or chemical attributes (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63; Fig. 1-3)* using the input data and the physical model to provide virtual sensor measurements relating to the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the virtual sensor measurements obtained *during the performance of the actual process* (Sonderman: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) to facilitate the *actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.7 Lines 37-65).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman

teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; *Col.7 Lines 8-20*), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7).

Regarding Claims 6-9

Sonderman teaches inputting *process* data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claim 11

Sonderman teaches repeating the step of inputting the data from (physical sensor) metrology tool into first principle simulation and facilitating the semiconductor

process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process (Sonderman: at least in Col.4 Lines 48-Col.5 Lines 10; Col.7 Lines 36-53; col.4-7).

Regarding Claims 13-14

Sonderman teaches performing first principle simulation not concurrently with the process performed; inputting data from at least one initial condition recorded from a previous process performed (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 17

Sonderman teaches using virtual sensor measurements to characterize the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 11-17; equipment model).

Regarding Claim 18

Sonderman teaches using virtual tool measurements to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 41-47).

Regarding Claim 19

Sonderman teaches using virtual sensor measurements to detect a fault in the process performed by the semiconductor-processing tool (Sonderman teaches: at least in Col.7, Fig 5-6).

Regarding Claims 21-25 (Updated)

Sonderman teaches using a network of interconnected resources *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the*

*factory floor – Col.9 Lines 60-65*) to perform *first principle simulation (Jain: Section III*) recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 26-27

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 28 (Updated)

System claim 28 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 29

System claim 29 discloses substantially similar limitations as method claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 30-32

System claims 30-32 disclose substantially similar limitations as method claims 3-5 and are rejected for the same reasons as claims 3-5.

Regarding Claims 33-36

System claims 33-36 disclose substantially similar limitations as method claims 6-9 and are rejected for the same reasons as claims 6-9.

Regarding Claim 37

System claim 37 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 38

System claim 38 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claims 40-41 and 61

System claims 40-41 and 61 disclose substantially similar limitations as method claims 13-14 and are rejected for the same reasons as claims 13-14.

Regarding Claim 44

System claim 44 discloses substantially similar limitations as method claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 45

System claim 45 discloses substantially similar limitations as method claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 46

System claim 46 discloses substantially similar limitations as method claim 19 and is rejected for the same reasons as claim 19.

Regarding Claims 48-52 (Updated)

System claims 48-52 disclose substantially similar limitations as method claims 21-25 and are rejected for the same reasons as claims 21-25.

Regarding Claims 53-54 (Updated)

System claims 53-54 disclose substantially similar limitations as method claims 26-27 and are rejected for the same reasons as claims 26-27. Dependency of claim 53 is changed from 48 to 28 and is noted by examiner.

Regarding Claim 55 (Updated)

System claim 55 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56

System claim 56 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 57

System claim 57 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claim 60

System claim 60 discloses substantially similar limitations as method claim 22 and is rejected for the same reasons as claim 22.

Regarding Claim 61

System claim 61 discloses substantially similar limitations as method claim 21 and is rejected for the same reasons as claim 21.

Regarding Claim 62

System claim 62 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 63-65

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

**13. Claims 12, 15-16, 20, 39, 42-43, 47, 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).**

Regarding Claim 12

Teachings of Sonderman & Jain are disclosed in claim 1 rejection above. Sonderman teaches setting boundary condition for first principle simulation through the process parameters (Sonderman: at least in Col.5-6).

Sonderman & Jain do not teach performing time dependent concurrent simulation without direct input from semiconductor process to facilitate semiconductor process based on virtual sensor measurement.

Chen teaches time dependent concurrent simulation without direct input from semiconductor process and applies the result to facilitate the semiconductor process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process. Chen teaches simulation based on the statistical data, which in turn provides the output to actual fabrication process (Chen: at least in Col.3 Lines 12-18).

Motivation to combine Jain to Sonderman is provided above in claim 1 rejection.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The

motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23). Chen facilitates in building the process model that can be run in parallel to actual process thereby providing more specific embodiment to Sonderman's teachings (Chen: Col.3 Lines 12-24).

Regarding Claim 15

Chen teaches indirectly putting best-known input parameters for the physical model (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 16

Chen teaches comparing virtual sensor measurements with the actual sensor measurements and refining at least one best known input parameters and the physical model to obtain better agreement between the virtual sensor measurements with actual sensor measurements (Chen: at least in Col.3 Lines 48-57; Calibrate run calibrate simulated).

Regarding Claim 20

Chen teaches storing virtual sensor measurement in a library for subsequent use in a first principle simulation (Chen: at least in Col.3; Specifically in Col.3 Lines 37-41).

Regarding Claim 39

System claim 39 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 42

System claim 42 discloses substantially similar limitations as method claim 15 and is rejected for the same reasons as claim 15.

Regarding Claim 43

System claim 43 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

Regarding Claim 47

System claim 47 discloses substantially similar limitations as method claim 20 and is rejected for the same reasons as claim 20.

Regarding Claim 58

System claim 58 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 59

System claim 59 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

---------- End of Rejection under 35 USC 103 ----------

***Conclusion***

4. All claims are rejected.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

***Communication***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akash Saxena/

KAMINI SHAH
SUPERVISORY PATENT EXAMINER